

FIG.1

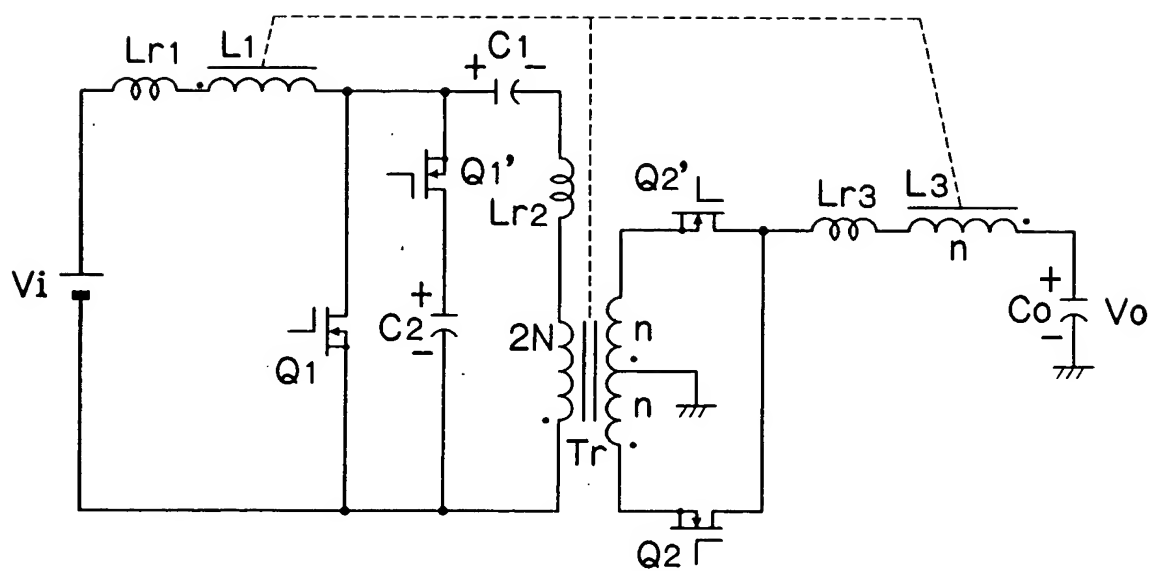


FIG.2

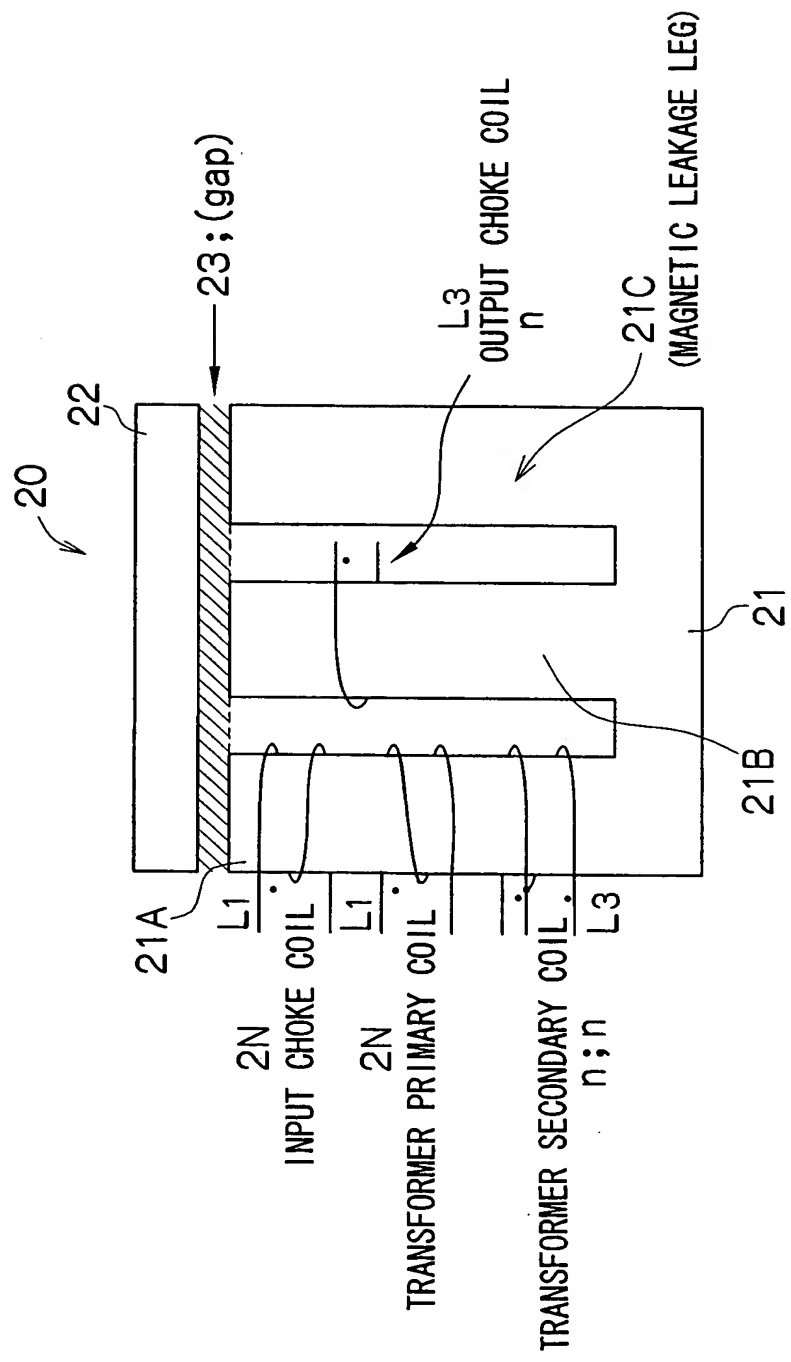


FIG.3

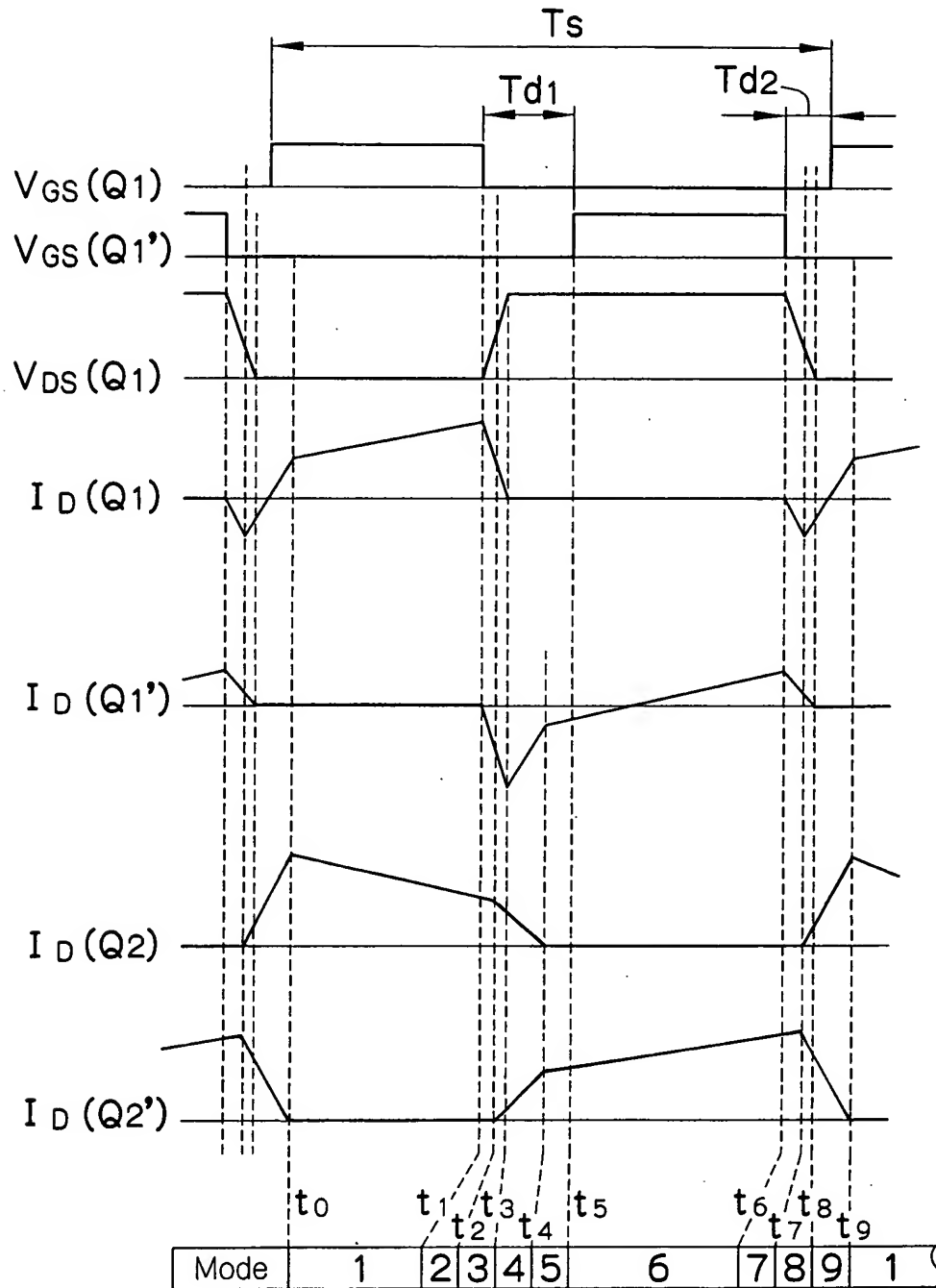


FIG.4

MODE 1

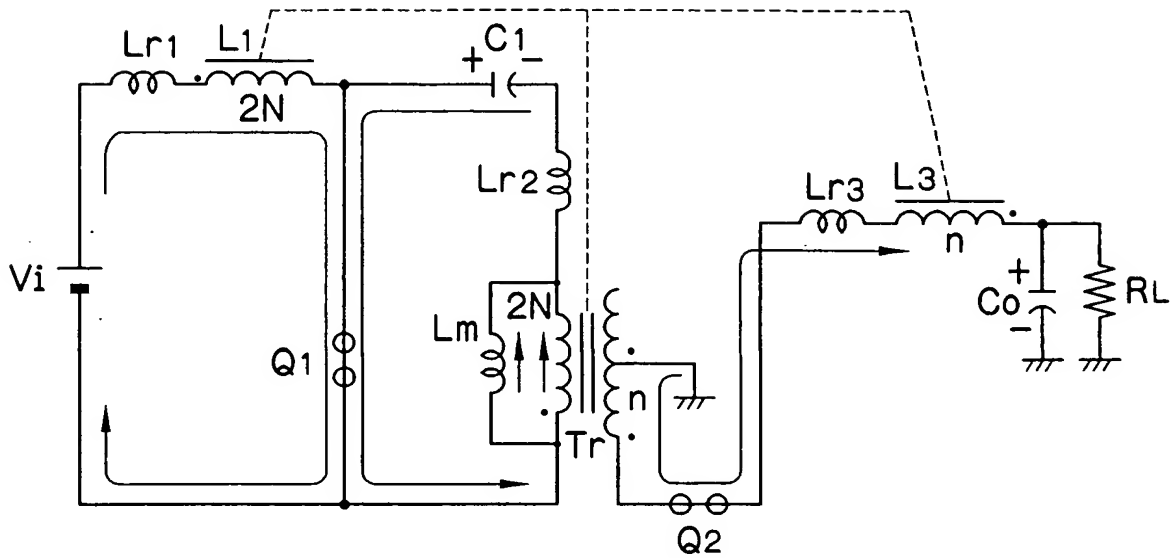


FIG.5

MODE 2

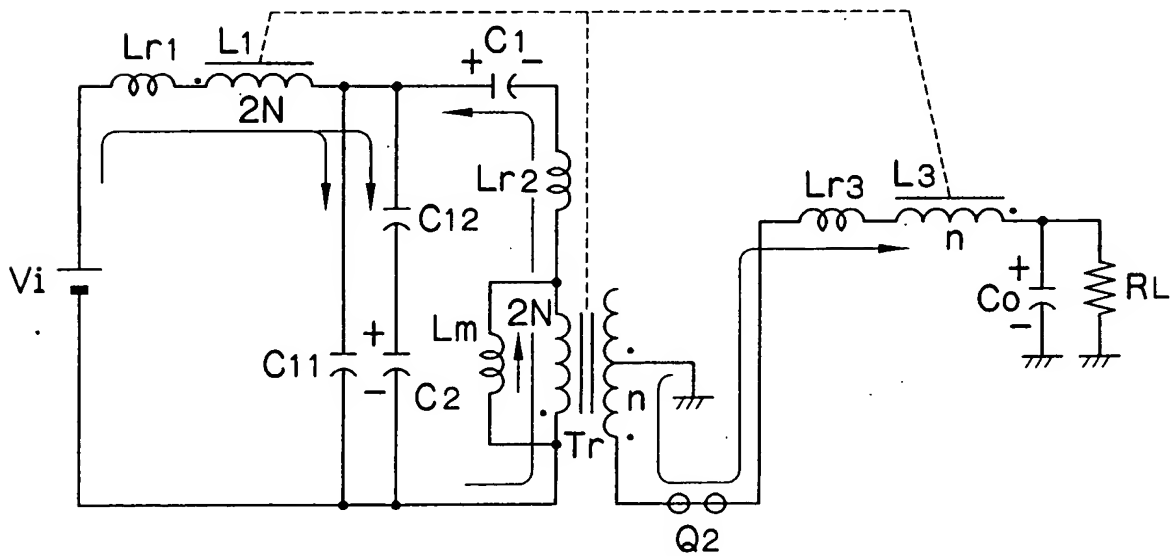


FIG.6

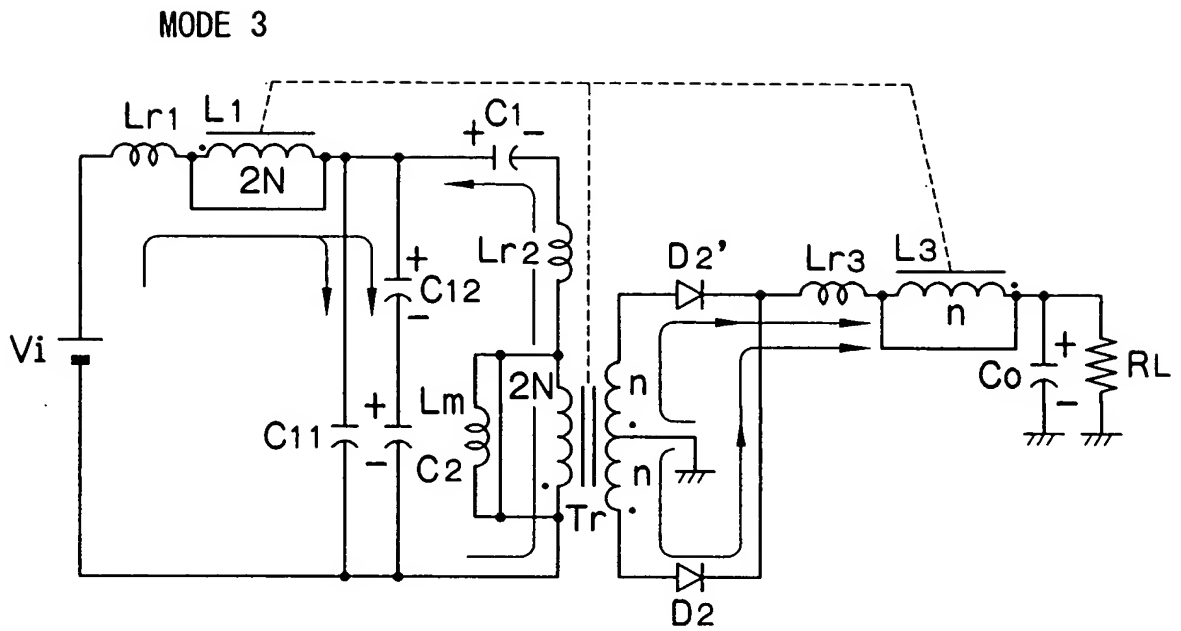


FIG.7

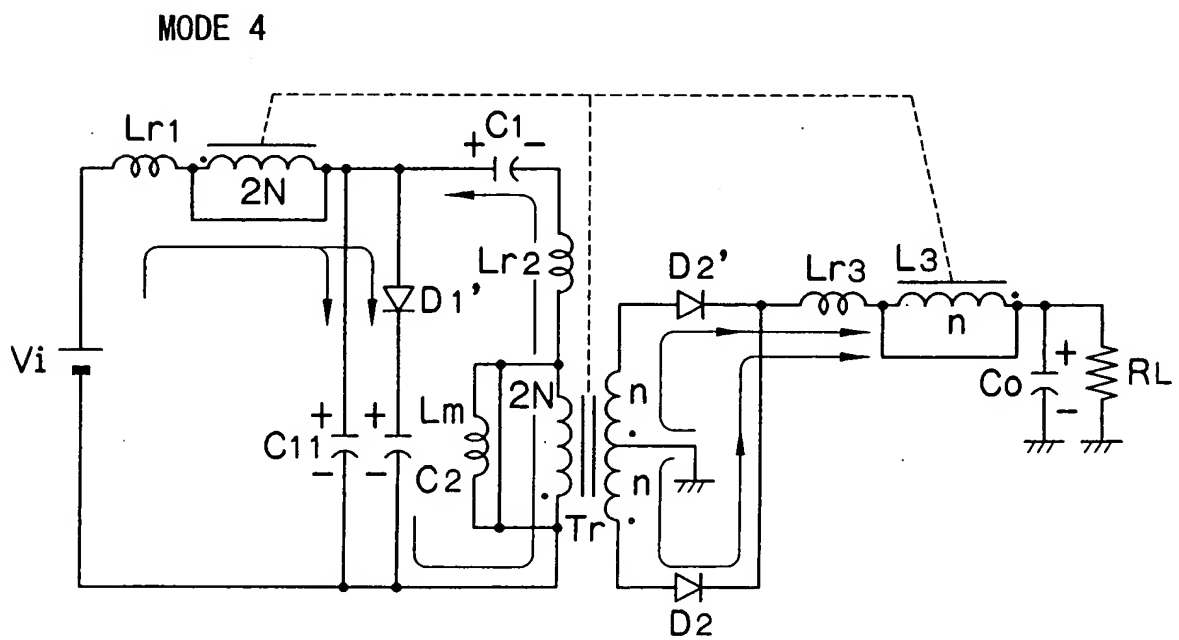


FIG.8

MODE 5

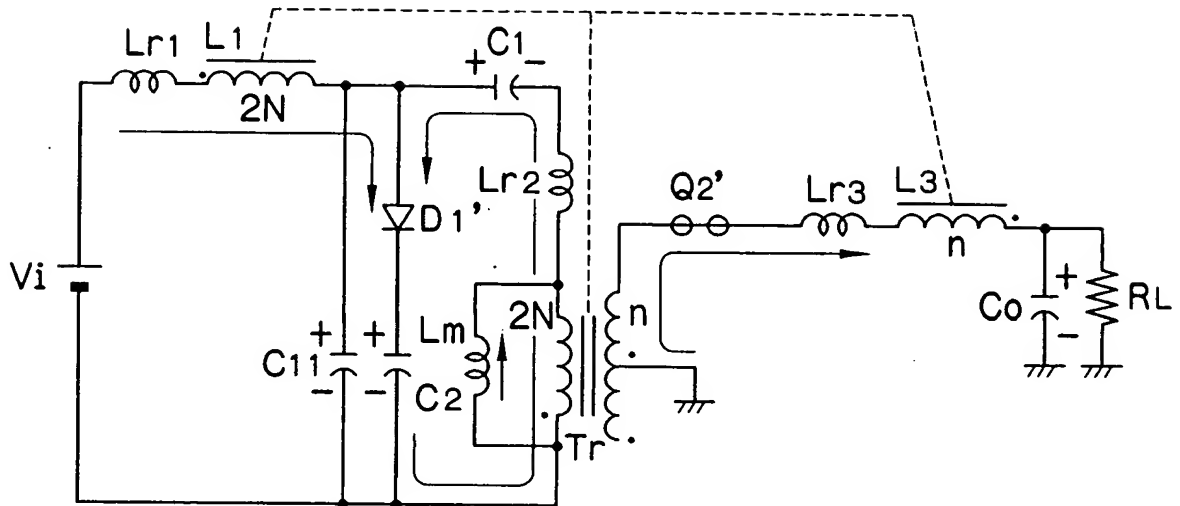


FIG.9

MODE 6

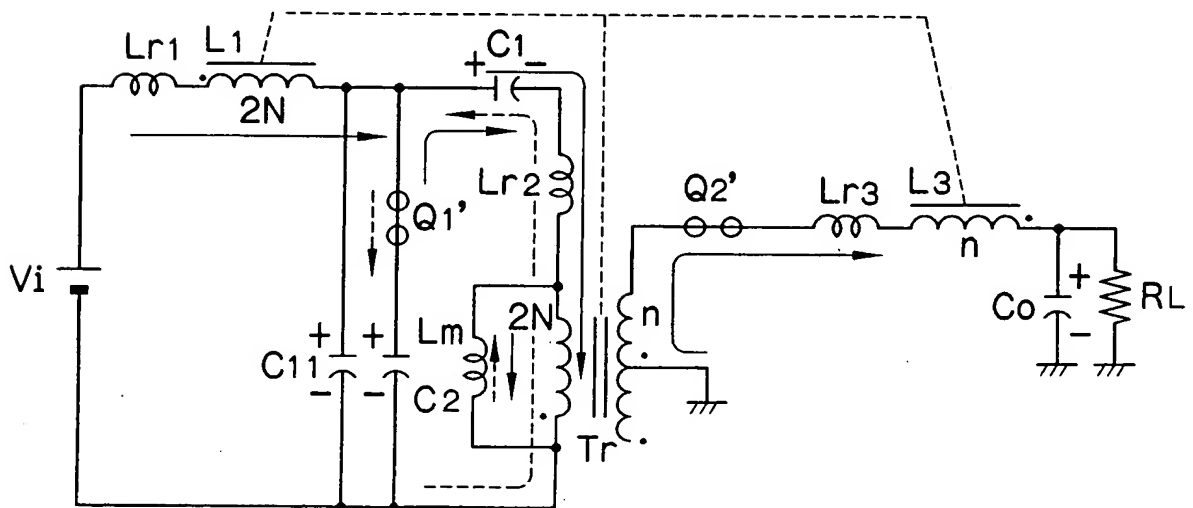


FIG.10

MODE 7

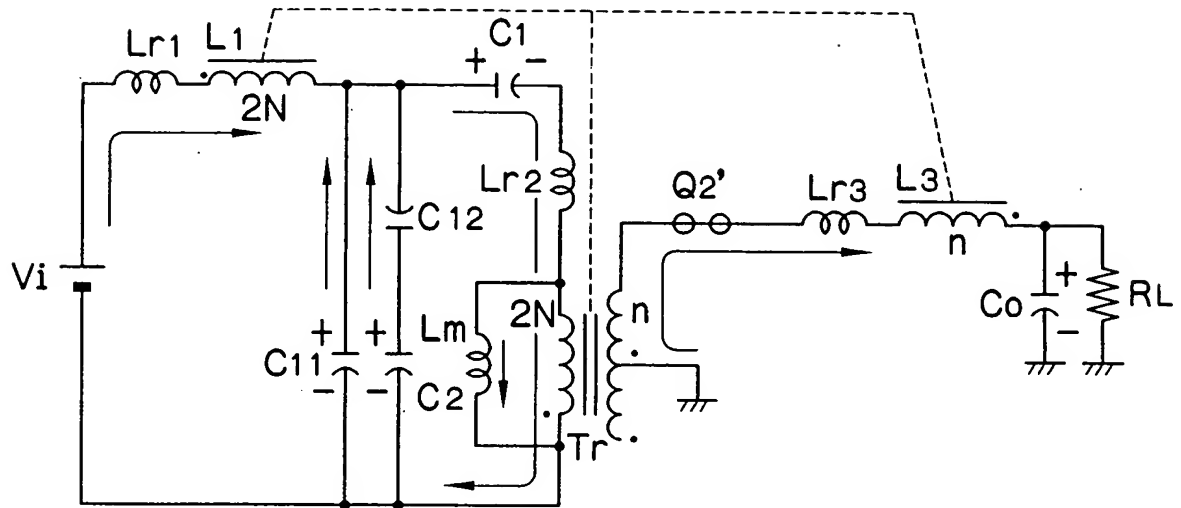


FIG.11

MODE 8

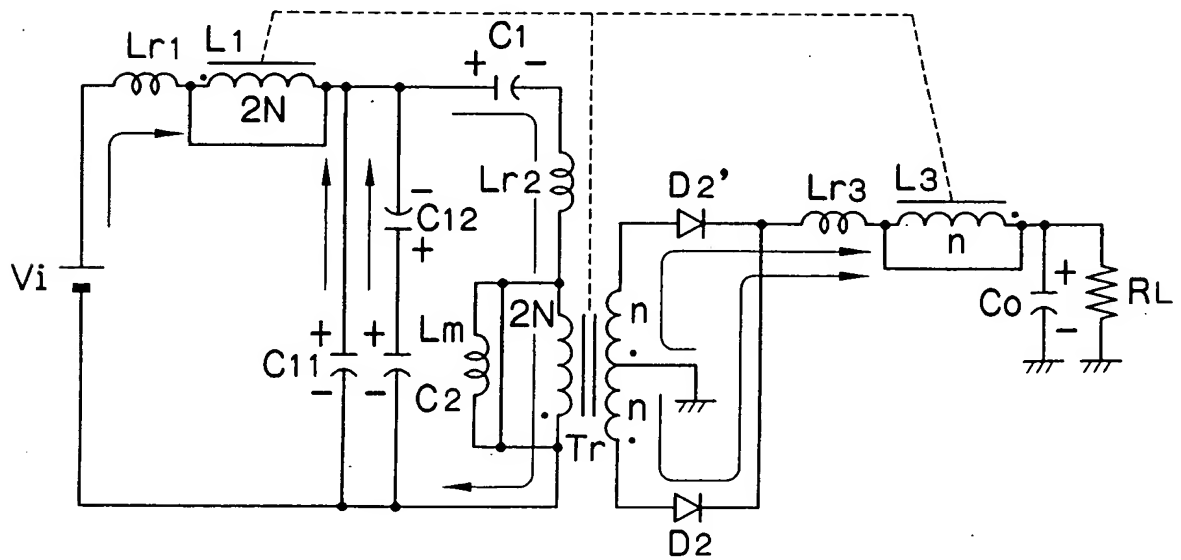
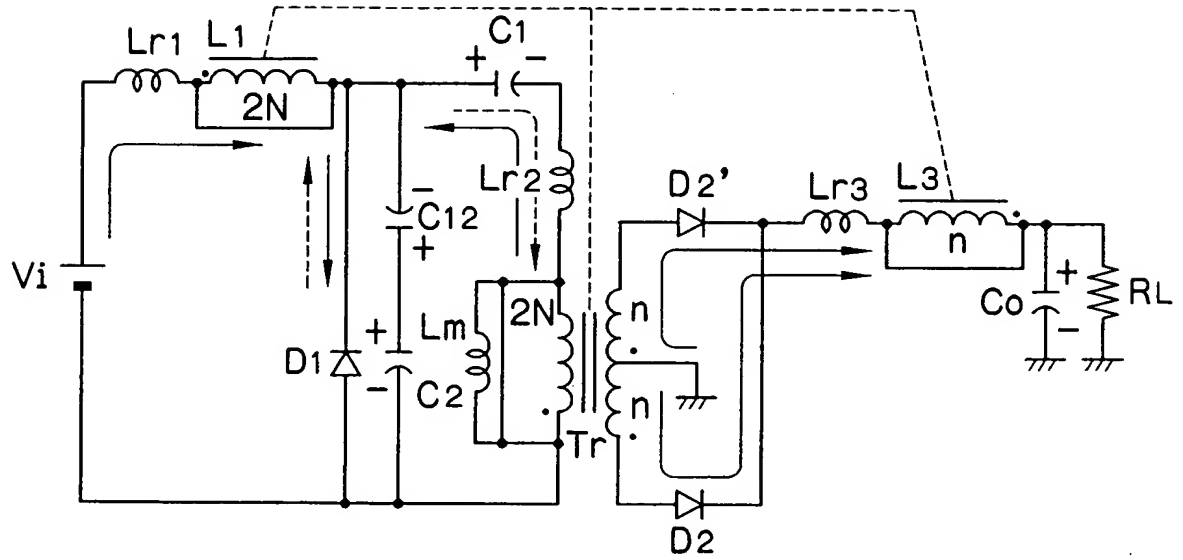


FIG.12

MODE 9





The diagram shows a Class-D push-pull amplifier. The input stage consists of a MOSFET driver (Q1, Q1') with a gate driver (Q2, Q2') and a transformer (Tr) with turns ratio 2N:n. The output stage is a push-pull MOSFET pair (Q2, Q2') driving a load (Lr3) through a transformer (Tr) with turns ratio n:n. The output is filtered by a low-pass filter (Lr1, Lr2, Lr3) and a capacitor (C1, C2, C3) to produce the output voltage (Vo). The input voltage is Vi.

FIG.15

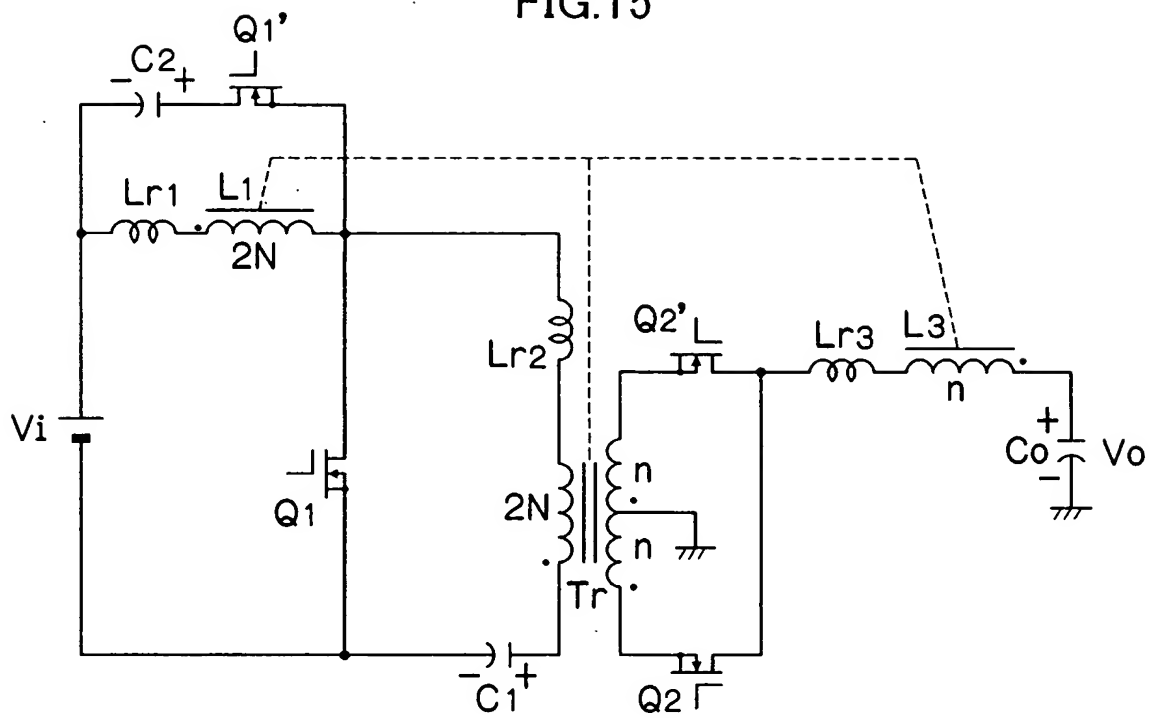


FIG.16

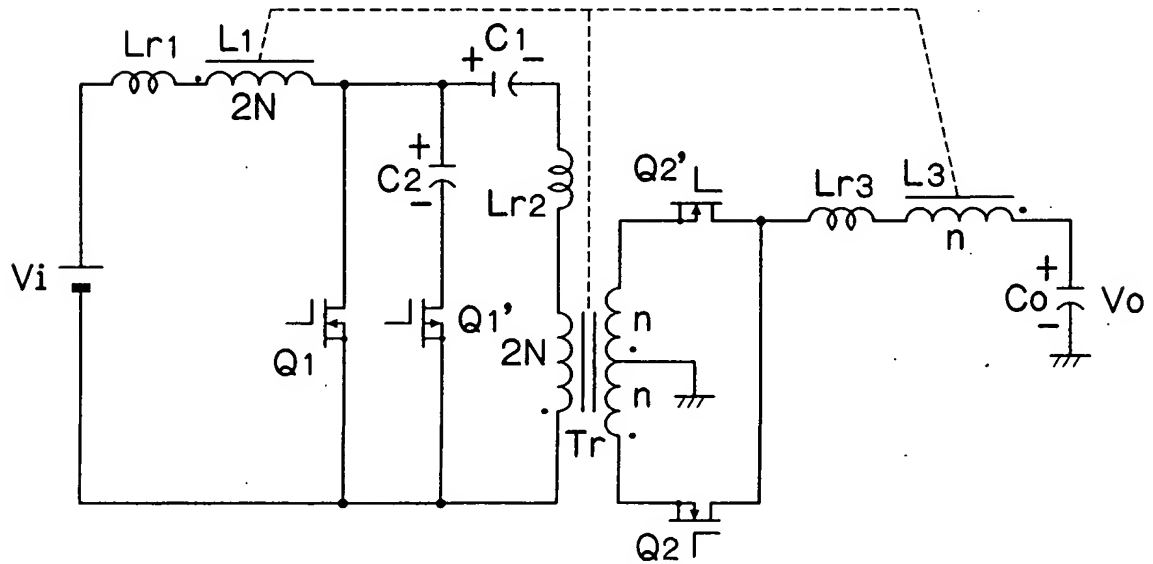


FIG.17

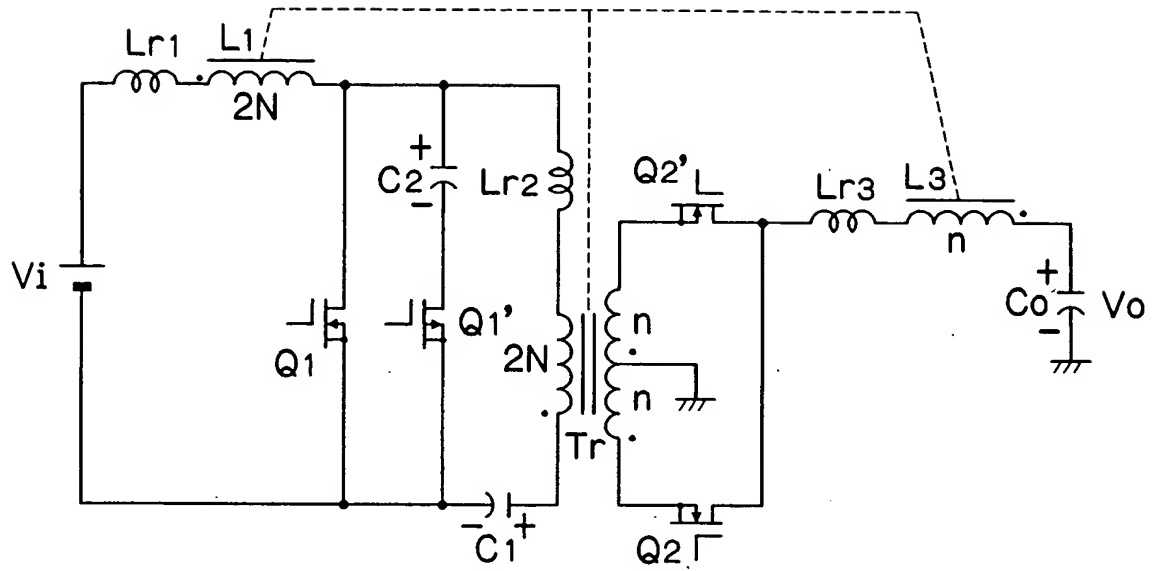


FIG.18

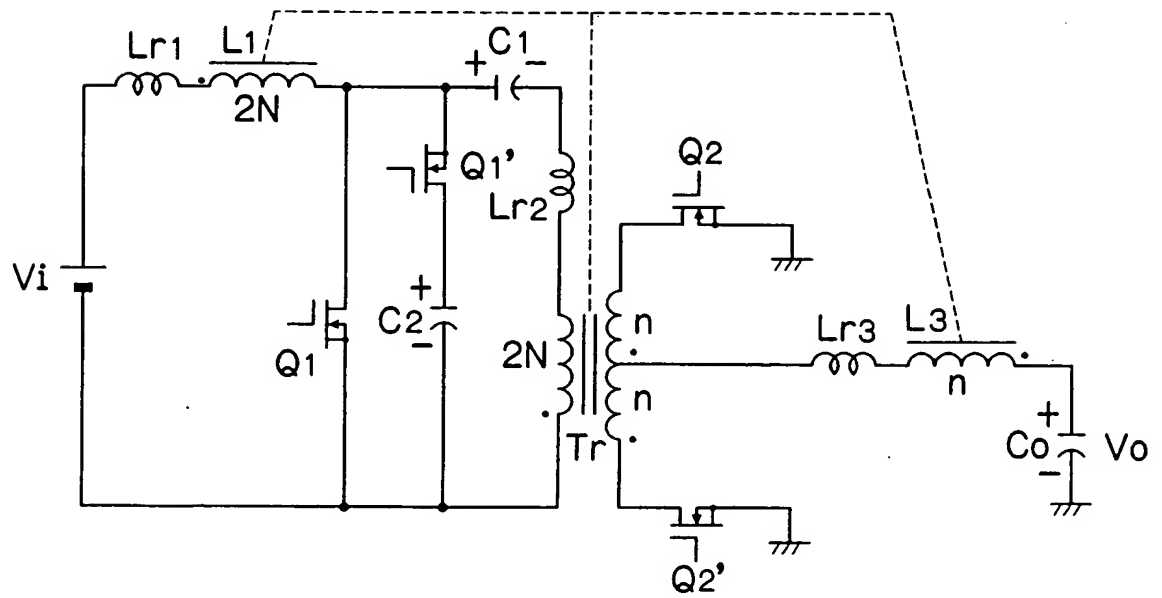


FIG.19

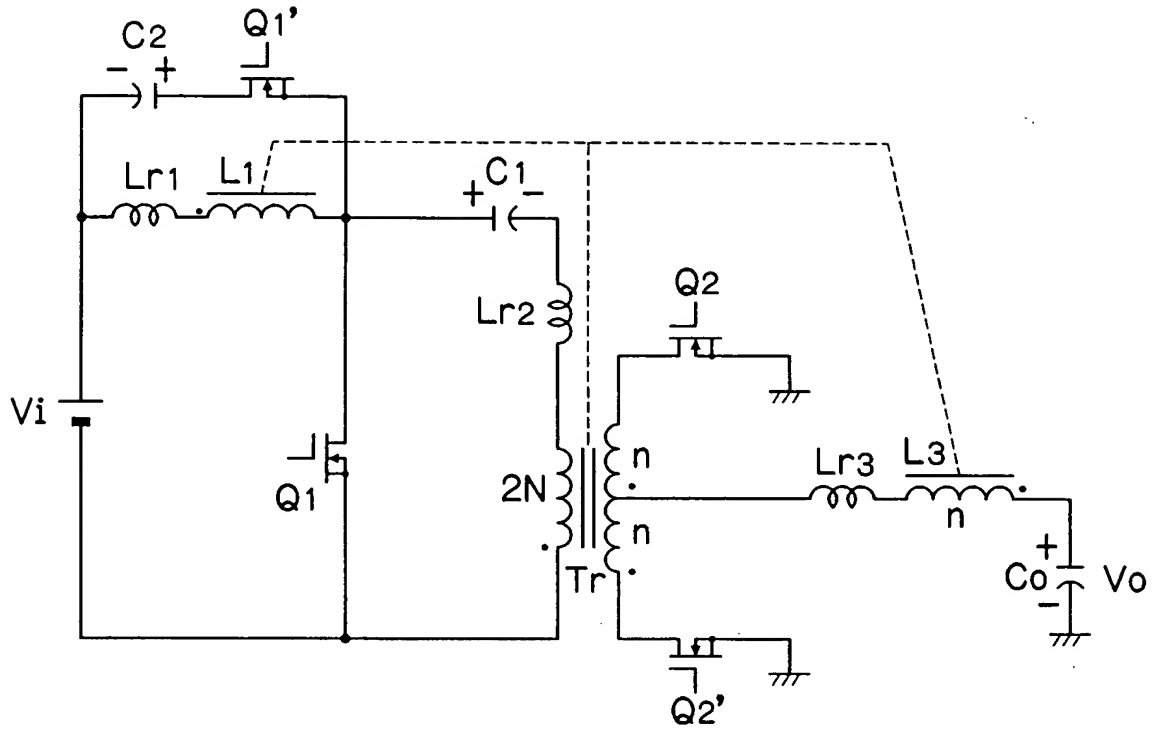
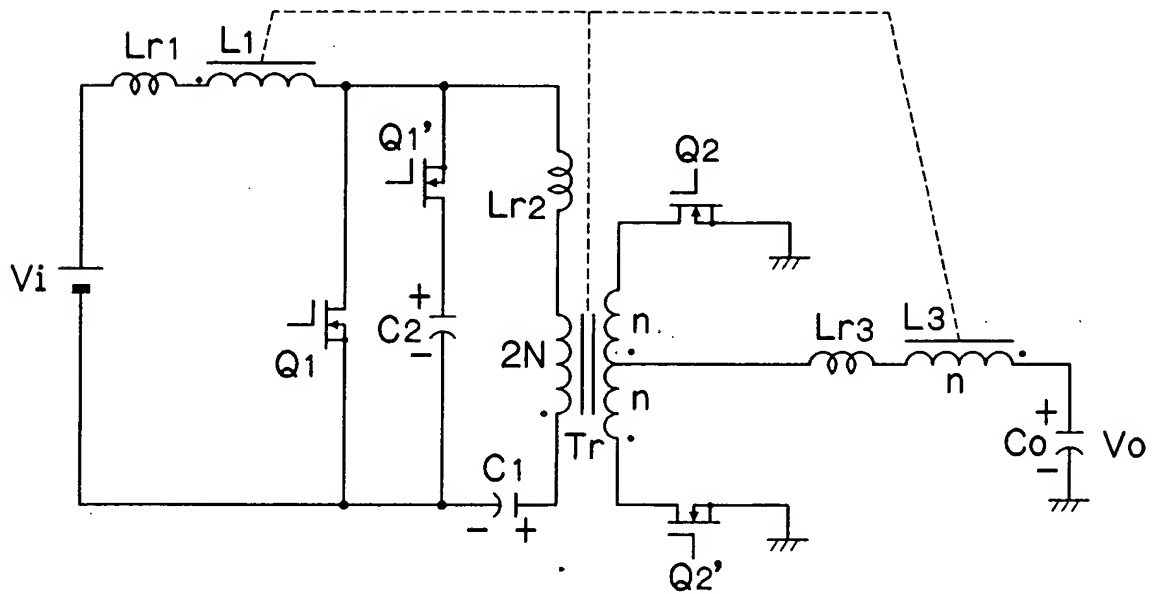


FIG.20



The diagram shows a full-bridge inverter circuit. The input DC voltage  $V_i$  is connected to a bridge consisting of four MOSFETs:  $Q1$  and  $Q1'$  on the left leg, and  $Q2$  and  $Q2'$  on the right leg. Each MOSFET has an anti-parallel capacitor ( $C1, C2$  for the left leg,  $C3, C4$  for the right leg). The bridge output is connected to a transformer  $Tr$  with primary inductance  $Lr1$  and secondary inductance  $Lr2$ . The transformer has a turns ratio of  $2N:n$ . The secondary is connected to a second-stage filter consisting of an inductor  $L3$  and a capacitor  $C5$  in parallel, which produces the output voltage  $V_o$ . A dashed line indicates a connection from the transformer secondary to the input of the second stage.

The diagram illustrates a two-stage power converter. The first stage is a buck converter consisting of an input voltage source  $V_i$ , an inductor  $L_{r1}$ , a diode  $L_1$ , a MOSFET  $Q_1$ , and a capacitor  $C_2$ . The second stage is a full-bridge inverter with MOSFETs  $Q_2$  and  $Q_2'$ , a transformer  $Tr$ , and an output filter inductor  $L_{r3}$ , diode  $L_3$ , and capacitor  $C_o$ . The output voltage is  $V_o$ . The transformer  $Tr$  has a turns ratio of  $n:n$ . The inductors  $L_1$  and  $L_3$  are connected to the output of the first stage and the input of the second stage, respectively. The capacitors  $C_1$  and  $C_2$  are connected to the input and output of the first stage, respectively. The MOSFETs  $Q_1$  and  $Q_2$  are driven by a common gate signal, while  $Q_2'$  is driven by an anti-parallel gate signal.

FIG.23

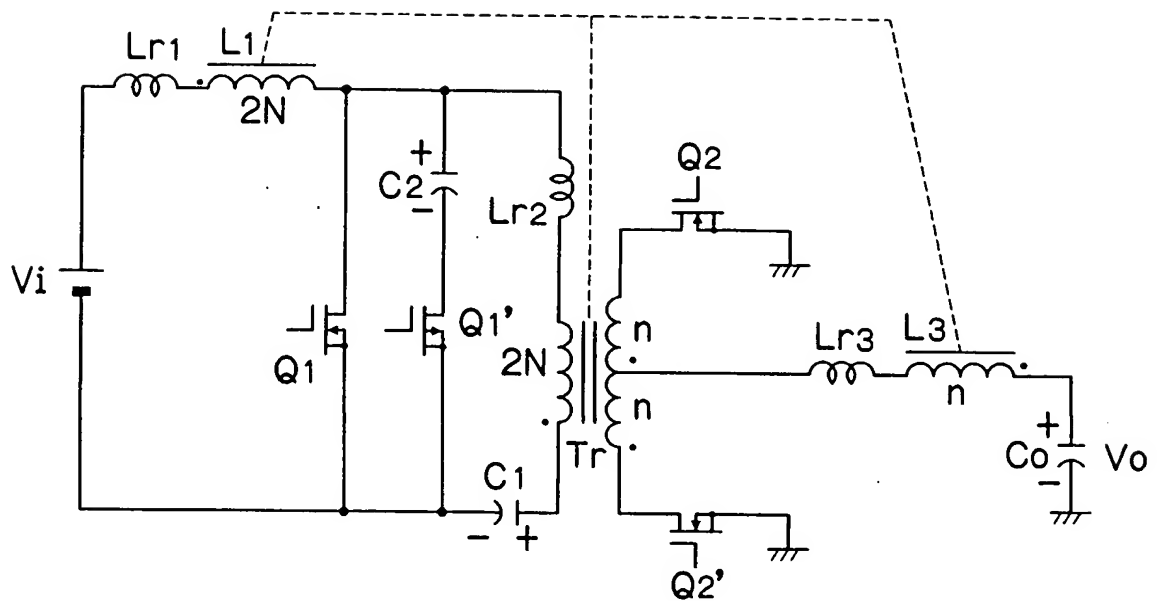
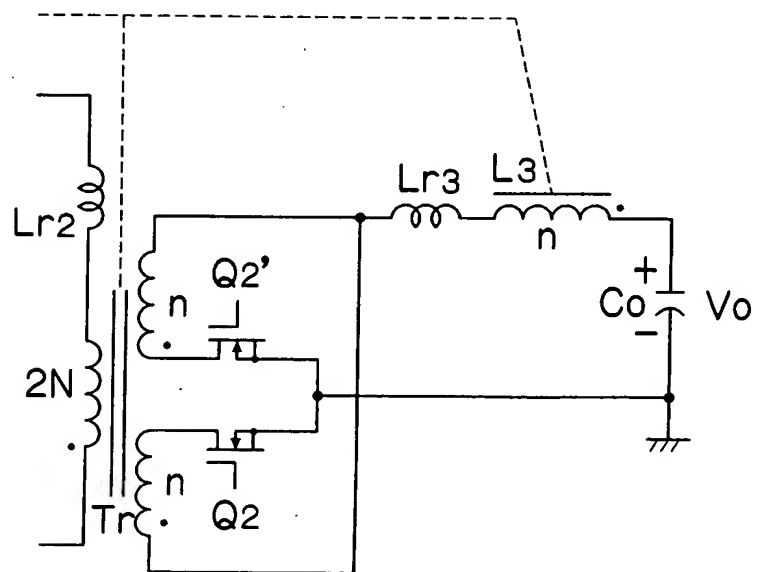
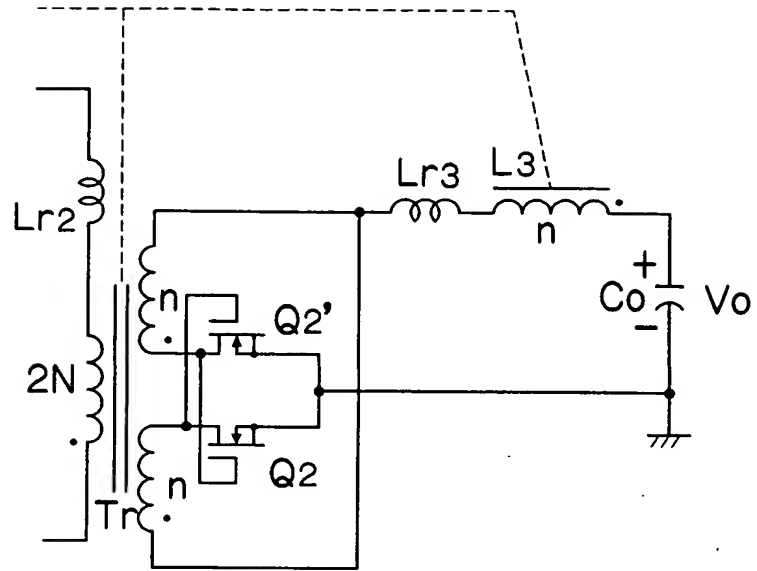


FIG.24



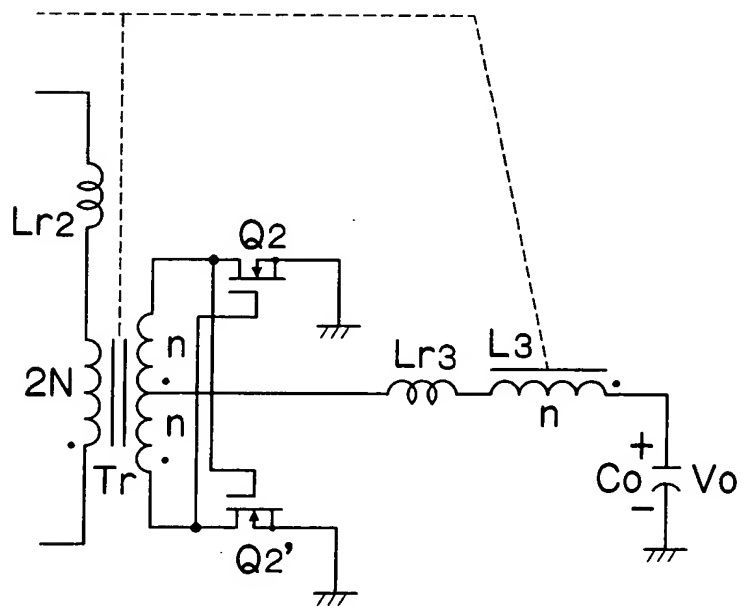
Tr PRIMARY CIRCUIT IS OMITTED

FIG.25



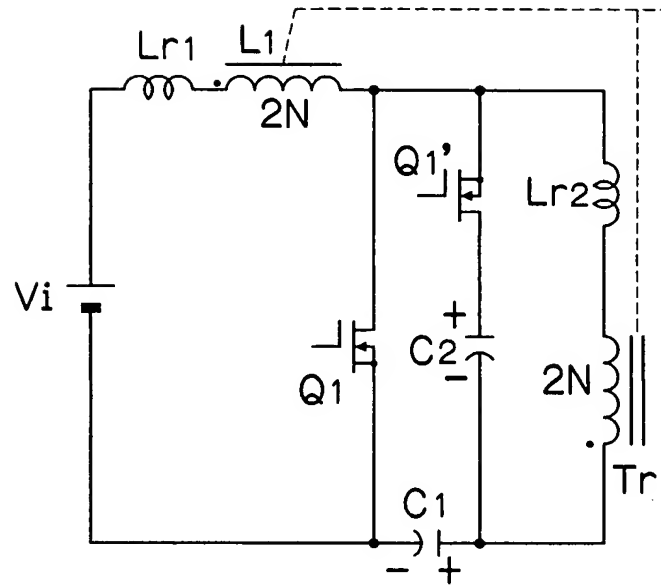
Tr PRIMARY CIRCUIT IS OMITTED

FIG.26



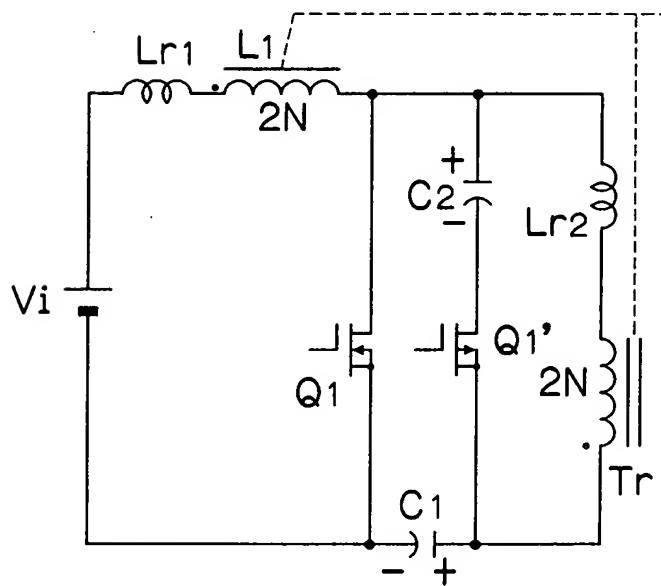
Tr PRIMARY CIRCUIT IS OMITTED

FIG.27



Tr SECONDARY CIRCUIT IS OMITTED

FIG.28



Tr SECONDARY CIRCUIT IS OMITTED



FIG.29  
PRIOR ART

